What is claimed is:

1. A frame synchronizing circuit comprising:

a synchronization pattern detecting unit that detects a first pattern and a second pattern each similar to a predetermined synchronization pattern in input data within a predetermined period of time;

a first frame synchronizing unit synchronizing with the first pattern at the first position of the input data;

a second frame synchronizing unit synchronizing with the second pattern at the second position of the input data; and

a first error detecting unit that detects that the first position is different from the position of the predetermined synchronization pattern,

and controls the first frame synchronizing unit to operate in accordance with the second position.

2. A frame synchronizing circuit according to claim 1, wherein

the synchronization by the first frame synchronizing unit and the synchronization by the second frame synchronizing unit differ from each other.

3. A frame synchronizing circuit according to claim 1, further comprising a second error detecting unit that detects that the second position is different from the position of the predetermined synchronization pattern,

wherein the synchronization pattern detecting unit detects a third pattern similar to the predetermined synchronization pattern in the input frame,

and controls the second frame synchronizing unit to operate in accordance with the third position.

4. A frame synchronizing circuit according to claim 1, wherein

the first error detecting unit detects that the first position is different from the position of the predetermined synchronization pattern based on information other than the

synchronization pattern in the frame.

5. A frame synchronizing circuit according to claim 4, wherein

the information includes a CRC code, and

when detecting the out-of-synchronization state of the frame continues for a predetermined period of time by using the CRC code, the first error detecting unit detects that the first position is not the position of the predetermined synchronization pattern.

6. A frame synchronizing circuit according to claim 1, wherein

the synchronization by the second frame synchronizing unit is selectively disabled by setting a predetermined mask.

7. A frame synchronizing circuit according to claim 1, further comprising a third error detecting unit that detects that the first position is different from the position of the predetermined synchronization pattern, based on a bit error with respect to the first pattern.

8. A frame synchronizing circuit comprising:

a synchronization pattern detecting unit that detects a plurality of patterns similar to a predetermined synchronization pattern in the input data within a predetermined period of time;

a plurality of frame synchronizing units each synchronizing with one of the plurality of patterns specified in order of detection at the position of the input data ; and

a first error detecting unit that detects that a first position of the plurality of positions is different from the position of the predetermined synchronization pattern,

and controls the frame synchronizing unit corresponding to the first position to operate in accordance with a second position of the plurality of positions other than the first position.

9. A frame synchronizing circuit according to claim 8, wherein

the positions of the plurality of patterns differ from each other.

10. A frame synchronizing circuit according to claim 8, further comprising a second error detecting unit that detects that the second position is different from the position of the predetermined synchronization pattern,

and controls the frame synchronizing unit corresponding to the first position to operate in accordance with a third position of the plurality of positions other than the first position and the second position.

11. A frame synchronizing circuit according to claim 8, wherein

the first error detecting unit detects that the first position is different from the position of the predetermined synchronization pattern based on information other than the synchronization pattern in the frame.

12. A frame synchronizing circuit according to claim 11, wherein

the information includes a CRC code and

when detecting the out-of-synchronization of the frame continues for a predetermined period of time by using the CRC code, the first error detecting unit detects that the first position is not the position of the predetermined synchronization pattern.

13. A frame synchronizing circuit according to claim 8, wherein

the synchronization by the plurality of frame synchronizing units are selectively disabled by setting a predetermined mask.

14. A frame synchronizing circuit according to claim 8, further comprising a third error detecting unit that detects that the first position is different from the position of the predetermined synchronization pattern, based on a bit error with respect to the first pattern.